POSITA 05020007

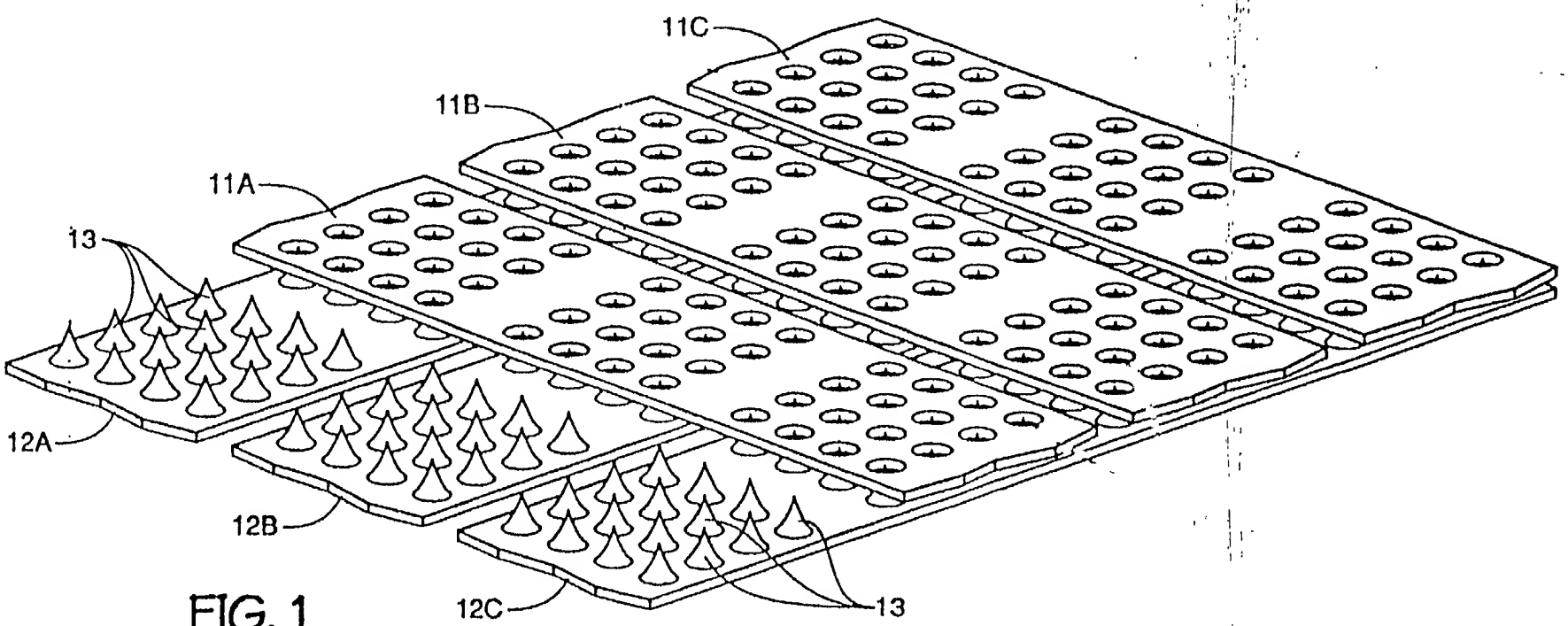


FIG. 1
(PRIOR ART)

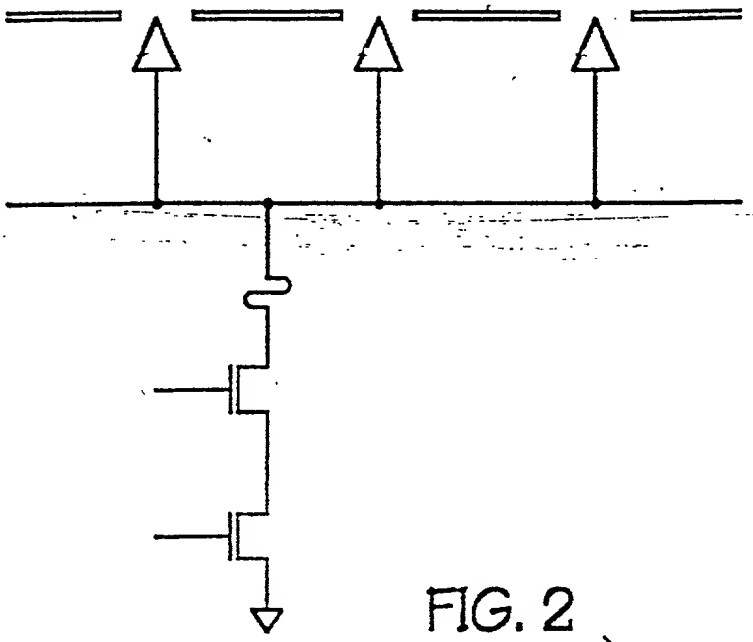


FIG. 2
(PRIOR ART)

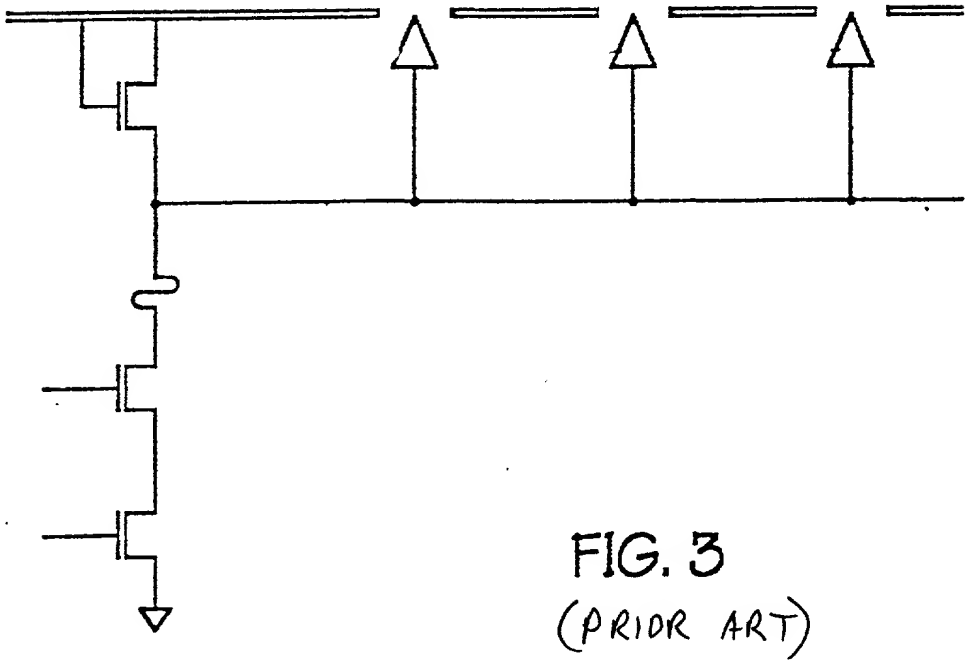


FIG. 3
(PRIOR ART)

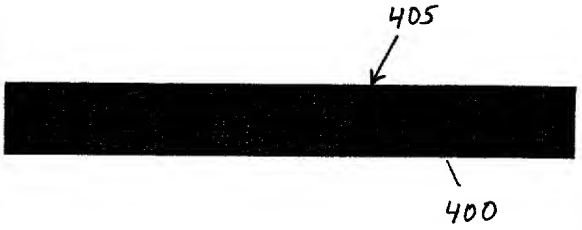
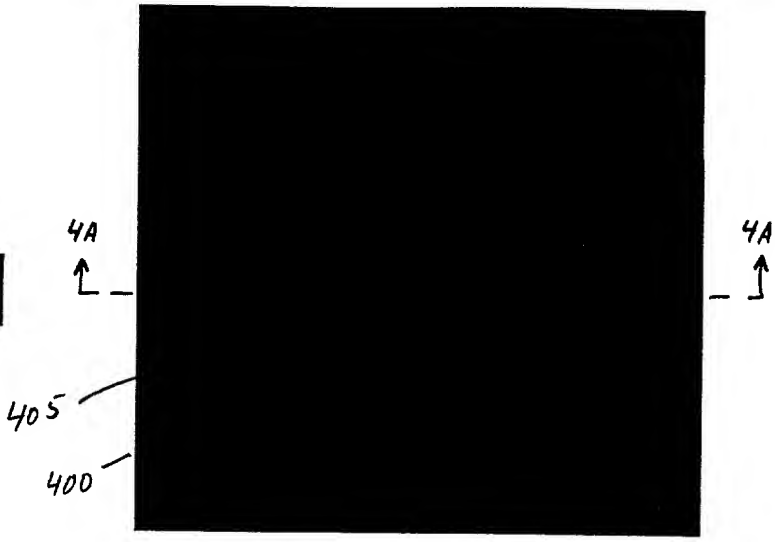


FIG. 4A



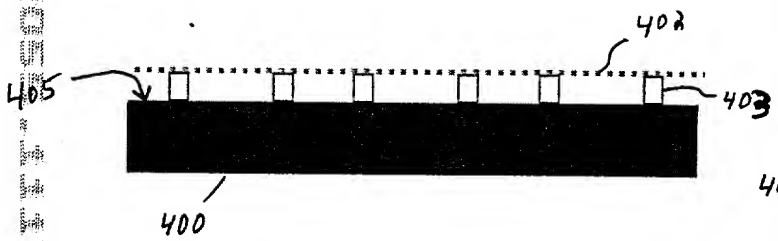
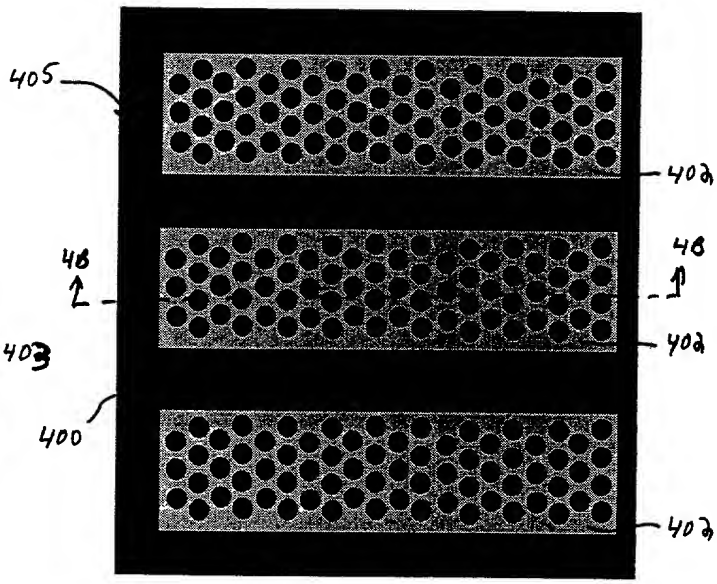


FIG. 4B



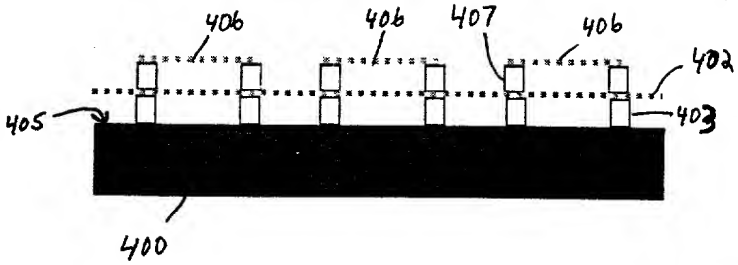
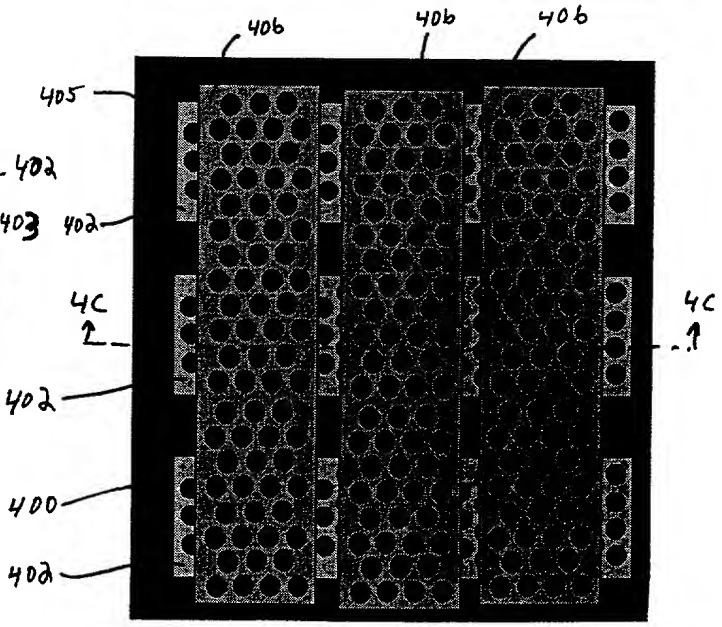


FIG. 4C



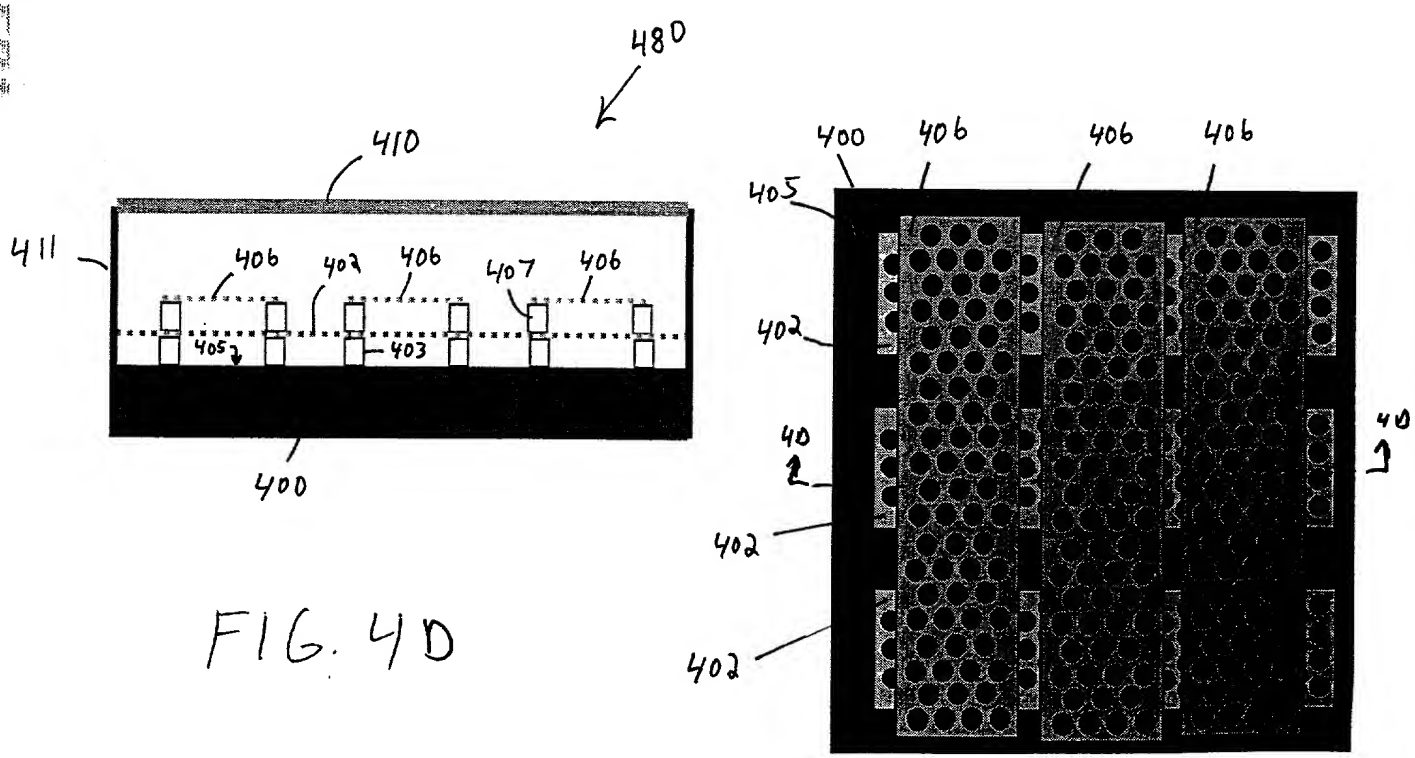

480
410
411
406
402
406
407
406
405
403
400
400
406
406
406
405
402
40
40
402
402

FIG. 4D

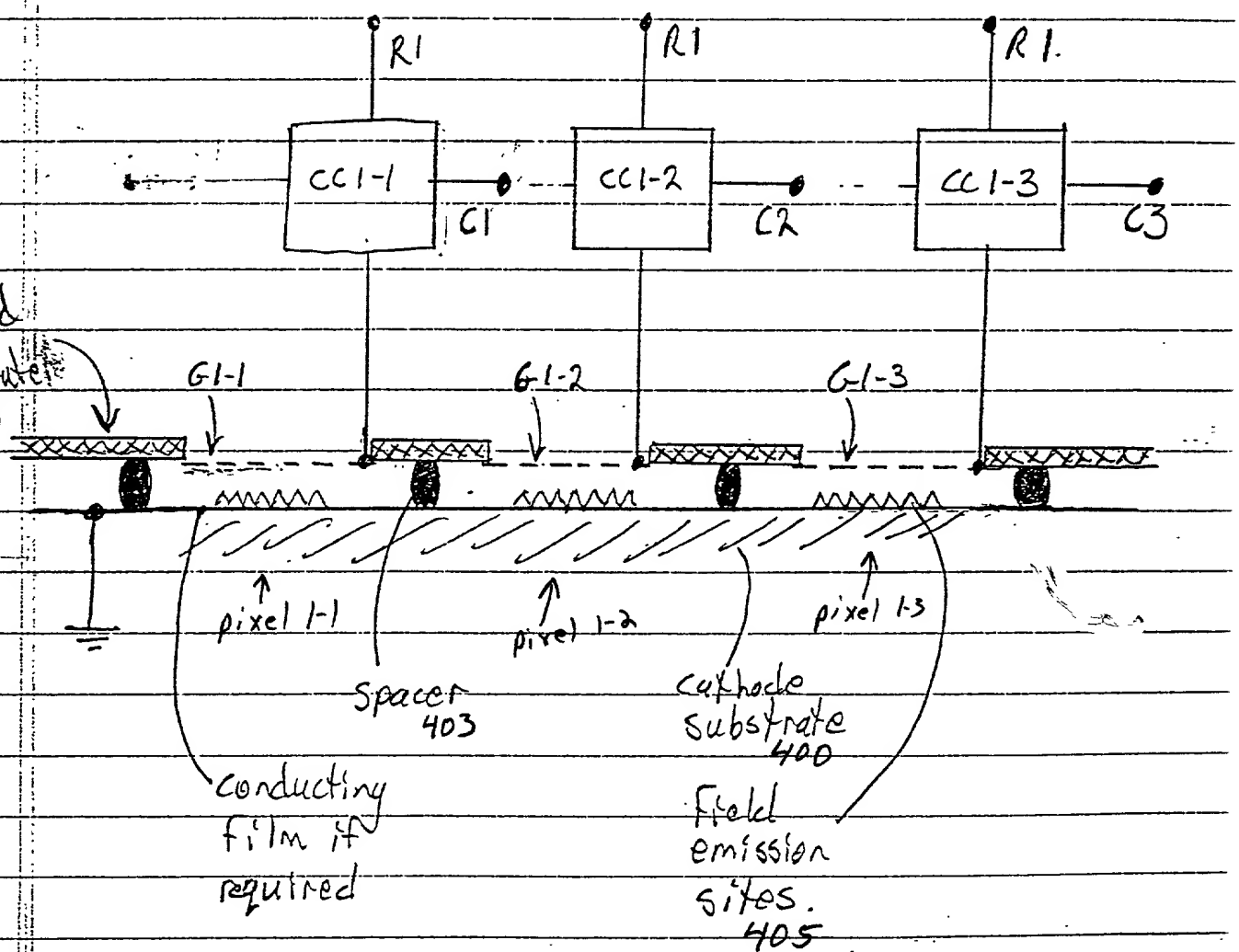

R1
R1
R1.
CC1-1
CC1-2
CC1-3
C1
C2
C3
grid substrate 402
G1-1
G1-2
G1-3
pixel 1-1
pixel 1-2
pixel 1-3
Spacer 403
cathode substrate 400
conducting film if required
Field emission sites. 405

Fig. 5

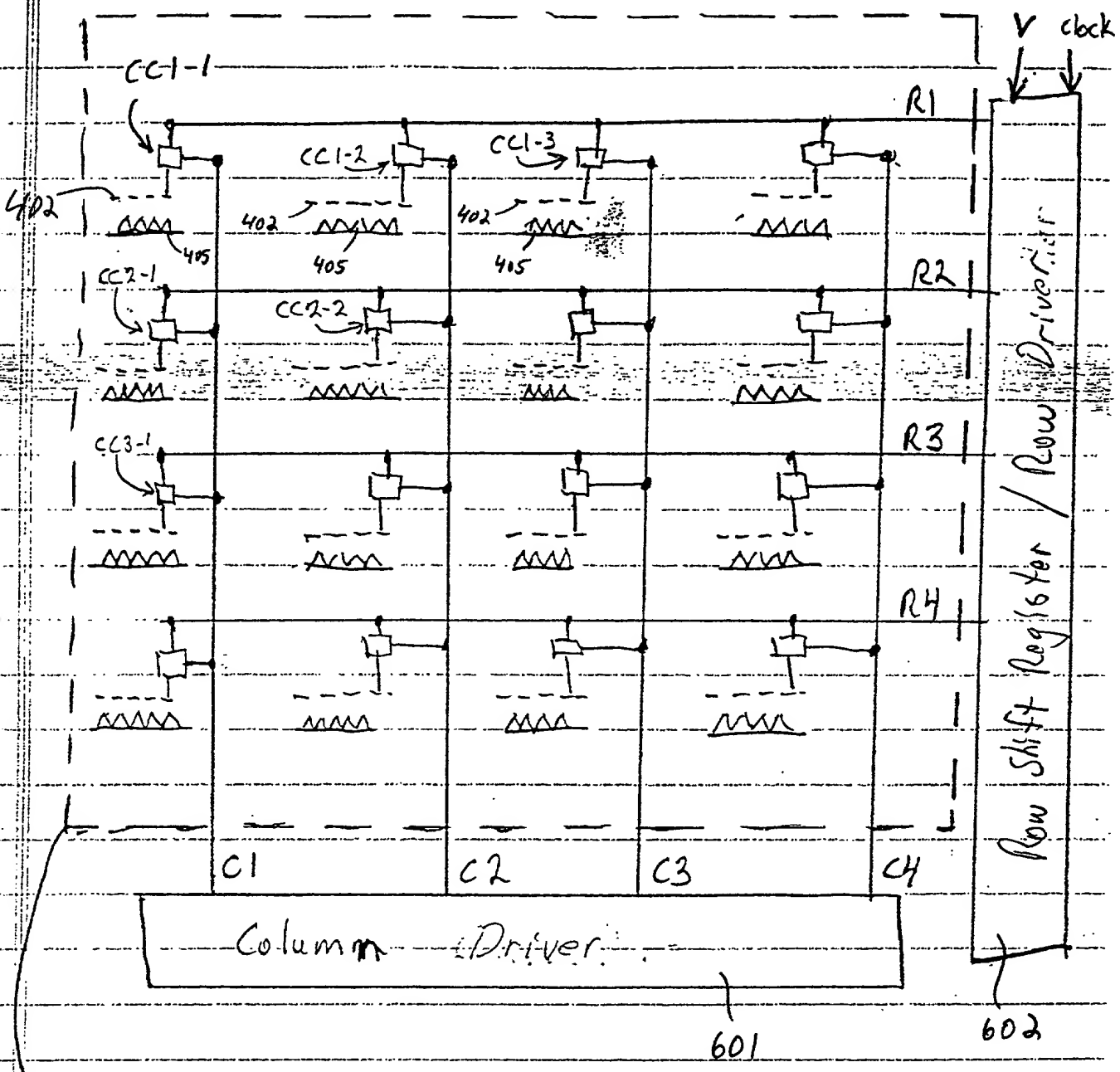

V clock
CC1-1
CC1-2
CC1-3
R1
R2
R3
R4
402
405
CC2-1
CC2-2
CC3-1
Row Shift Register / Row Driver
C1
C2
C3
C4
Column Driver
601
602
Active grid 600

Fig. 6.

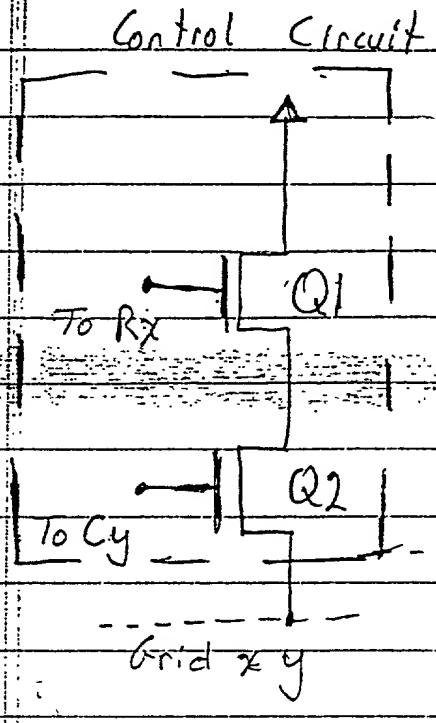

Control Circuit x y
Q1
To Rx
Q2
To Cy
Grid x y

Fig. 7

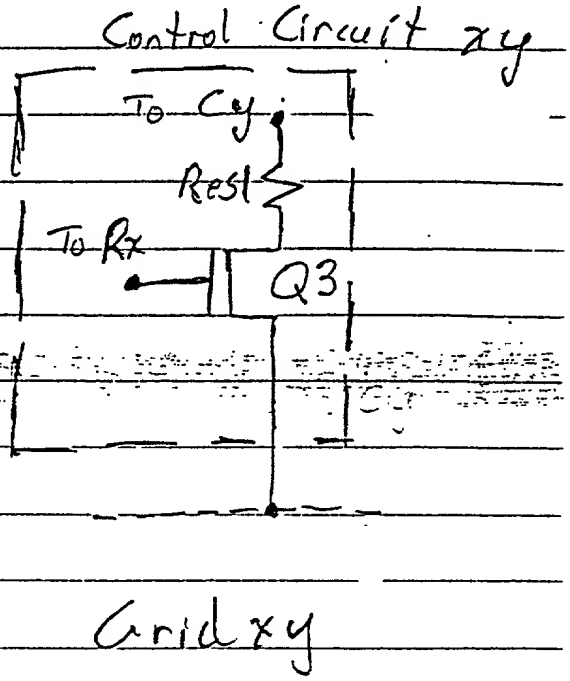

Control Circuit x y
To Cy
Rest
To Rx
Q3
Grid x y

Fig. 8

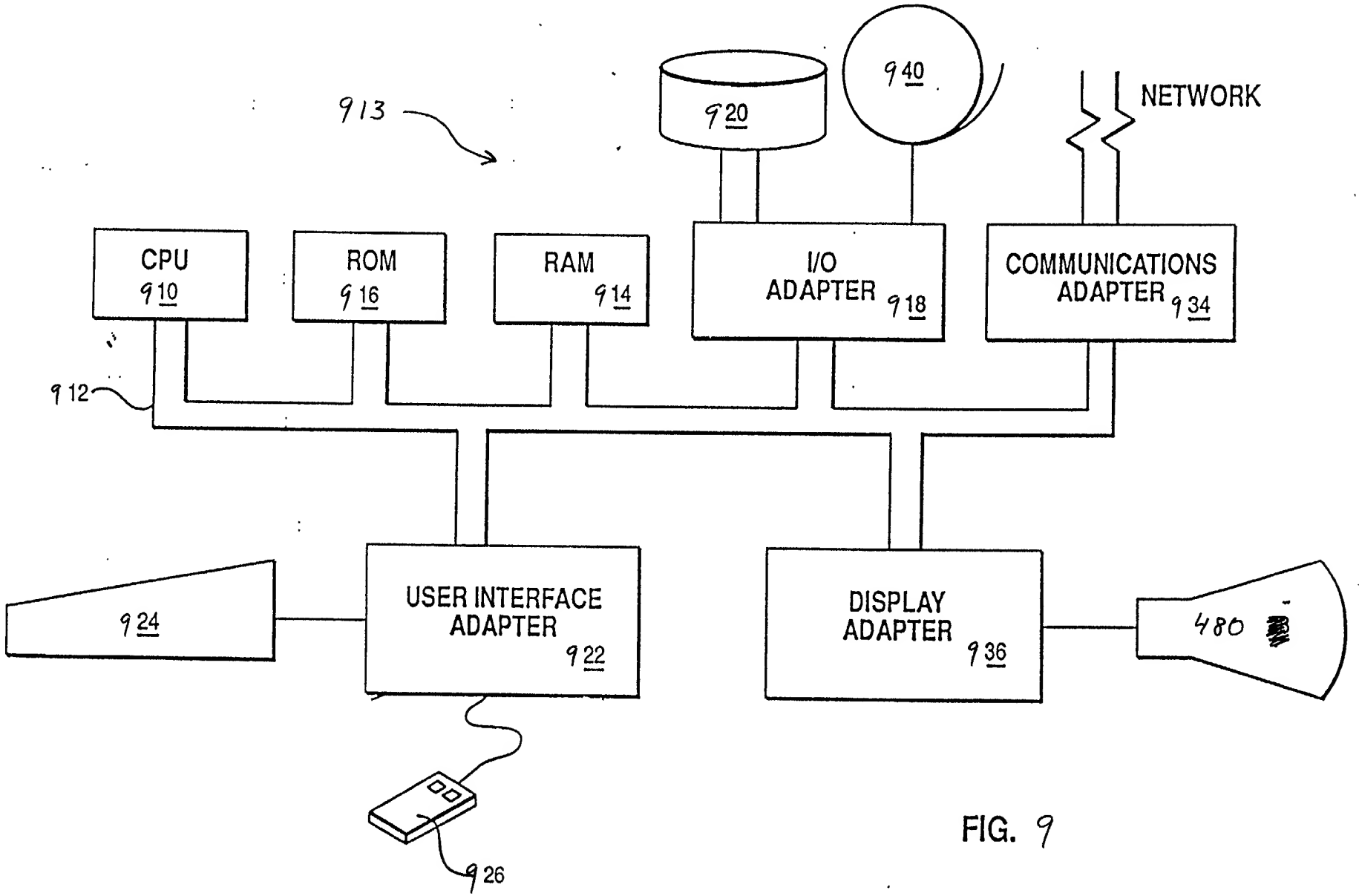

913
920
940
NETWORK
CPU
910
ROM
916
RAM
914
I/O
ADAPTER
918
COMMUNICATIONS
ADAPTER
934
912
924
USER INTERFACE
ADAPTER
922
DISPLAY
ADAPTER
936
480
926

FIG. 9